QUESTION BANK

Name of the Department : **Electrical and Electronics Engineering**

Subject Code & Name : **EE8351 & Digital Logic Circuits**

Year & Semester : **II & III**

UNIT I SYSTEMS COMPONENTS AND THEIR REPRESENTATION

PART-A

1. Where the digital systems are used?
Digital systems are used extensively in computation and data processing, control systems, Communications and measurements. Since digital systems are capable of greater accuracy and reliability than analog systems, many tasks formerly done by analog are now being performed digitally.

2. What is the difference between analog and digital systems?
In a digital system the physical quantities or signals can assume only discrete values, while in analog systems the physical quantities or signals vary continuously over a specified range.

3. What is a binary number system and Why are binary numbers used in digital systems?
The number system with base (or radix) two is known as the binary number system. Only two symbols are used to represent the numbers in the system and these are 0 and 1.The outputs of the switching devices used in digital systems assume only two different values. Hence it is natural to use binary numbers internally in digital systems.

4. What is the difference between binary code and BCD?
Binary:
i. Any distinct element can be represented by a binary code.
ii. No limitation for the minimum or maximum number of elements required for coding the element.
BCD:
i. Only a decimal digit can be represented.
ii. It is a four bit representation.

5. What is an Excess3 code?

The excess3 code is a non weighted code which is obtained from the 8-4-2-1 code by adding 3(0011) to each of the codes.

6. What is a gray code and mention it.s advantages.

A gray code is a non weighted code which has the property that the codes for successive decimal digits differ in exactly one bit. The gray code is used in applications where the normal sequence of binary numbers may produce an error during the transition from one number to the next.

7. What is meant by non-weighted codes?

Each bit has no positional value i). Excess-3 code ii).Gray code iii).Five bit BCD

8. What is depletion mode& enhancement mode operation MOS?

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode. If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

9. List the names of universal gates. Why it is named so?

NAND and NOR gates are universal gates. Because a combination of NAND gates or a combination of NOR gates can be used to perform functions of any of the basic logic gates.

10. What is mean by Fan out?

Number of logic gates at the next stage that can be loaded to a given logic gate output so that voltages for each of the possible logic state remain within the defined limits.

11. What is propagation delay?

Propagation delay for a logic output from a logic gate means the time interval between change in a defined reference point input voltage and reflection of its effect at the output. It can also be defined as the time interval between changes in a defined logic level input and reflection of its effect at the output logic level.

12. What is noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output.It is expressed in volts.

13.Explain the procedure for BCD addition?

In BCD addition of two numbers involve following rules:-

1. Maximum value of the sum for two digits = 9 (max digit 1) + 9 (max digit 2) + 1 (previous addition carry) = 19

2. If sum of two BCD digits is less than or equal to 9 (1001) without carry then the result is a correct BCD number.

3. If sum of two BCD digits is greater than or equal to 10 (1010) the result is in-correct BCD number. Perform steps 4 for correct BCD sum.
4. Add 6 (0110) to the result.

14.Explain the procedure for excess-3 code?

Excess-3 code is an example of unweighted code. Excess-3 equivalent of a decimal number is obtained by adding 3 and then converting it to a binary format. For instance to find excess-3 representation of decimal number 4, first 3 is added to 4 to get 7 and then binary equivalent of 7 i.e. 0111 forms the excess-3 equivalent.

15.What do you understand by self complementing code?

A binary code is self complementary if complement of any code word is again a code .in self completing codes 9's complement of a number can be obtained by interchanging 0's and 1's.

16.Why the Gray code is called as reflected binary code?

This is a variable weighted code and is cyclic. This means that it is arranged so that every transition from one value to the next value involves only one bit change. The gray code is sometimes referred to as reflected binary, because the first eight values compare with those of the last 8 values, but in reverse order.

17. What is meant by non-weighted codes?

Each bit has no positional value i). Excess-3 code ii).Gray code iii).Five bit BCD

18. State advantages and disadvantages of TTL.

Adv:
. Easily compatible with other ICs
. Low output impedance
Disadv:
. Wired output capability is possible only with tristate and open collector types
. Special circuits in Circuit layout and system design are required.
. Masked ROM.
. Programmable Read only Memory
. Erasable Programmable Read only memory.
. Electrically Erasable Programmable Read only Memory.

19. Classify the logic family by operation?

The Bipolar logic family is classified into Saturated logic, Unsaturated logic. The RTL, DTL, TTL, I2L, HTL logic comes under the saturated logic family. The Schottky TTL, and ECL logic comes under the unsaturated logic family.

20. Mention the classification of saturated bipolar logic families.

The bipolar logic family is classified as follows:
RTL- Resistor Transistor Logic, DTL- Diode Transistor logic, I2L- Integrated Injection Logic.TTL- Transistor Transistor Logic, ECL- Emitter Coupled Logic.

21. Mention the important characteristics of digital IC.s?

Fan out, Power dissipation, Propagation Delay, Noise Margin , Fan In, Operating temperature ,Power supply requirements.

22. Convert the hexadecimal number E3FA to binary. (Nov 2007)

Solution:

E3FA16 – Hexadecimal
E 3 F A
11102 00112 11112 10102
So the equivalent binary value is 11100011111110102

23. Perform the following conversion (1029)10 to gray (May 2006)

Solution:

1 0 2 9 ----- Decimal
0001 0000 0010 1001 ----- BCD
0001 0000 0011 1101 ----- Gray
Thus the Gray code of 102910 is 00010000001111012

24. Add 1A816 and 67B16 (EE Nov 2004)

Solution:

1 A 816
6 7 B16
---
8 2 316

= 82316

PART-B

1. Explain the concept of working of RTL logic families.
2. Explain the working of DTL logic families.
3. Explain the concept, working and characteristics of TTL logic families.
4. Design a TTL logic circuit for a 3 input NAND gate.
5. With circuit schematic explain the working of a two-input TTL NAND gate.
6. With circuit schematic explain the operation of a two input TTL NAND gate.
7. Explain NOR and OR gate construction using ECL.Also give the characteristics of ECL family.
8. a. Explain the formation inverter using CMOS and its operation.
b. Discuss the characteristics of ECL circuit.
9. a. Explain the working of two inputs CMOS NAND gate.
b. Compare the performance of various logic families.
10. a. Write notes on the digital logic families comparing the characteristics.
b. Explain the working of two inputs TTL NAND gate.

UNIT II COMBINATIONAL CIRCUITS

PART-A

1.What are called don't care conditions?
In some logic circuits certain input conditions never occur, therefore the Correspondingoutput never appears. In such cases the output level is not defined, it can be either high or low.These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

2.What is a prime implicant?
A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

3.What is an essential implicant?
If a min term is covered by only one prime implicant, the prime implicantis said to be Essential.

4.**Define combinational logic.**
When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

5.Write the design procedure for combinational circuits.
The problem definition
xDetermine the number of available input variables & required O/P variables.xAssigning letter symbols to I/O variables
xObtain simplified Boolean expression for each O/P.
xObtain the logic diagram.

6.Define half adder and full adder.
The logic circuit that performs the addition of two bits is a half adder. The circuit that Performs the addition of three bits is a full adder

7.Define Decoder
A decoder is a multiple -input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

8.What is binary decoder?
A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

9.DefineAn encoder has 2n input lines and n output lines.
In encoder the output lines generate the binary code corresponding to the input value.

10.What is priority Encoder?
A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest prioritywill take precedence.

11.Define multiplexer.
Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

12.What do you mean by comparator?
A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

13.Write down the steps in implementing a Boolean function with levels of NAND Gates.
xSimplify the function and express it in sum of products.
xDraw a NAND gate for each product term of the expression that has at least two Literals.

xThe inputs to each NAND gate are the literals of the term.
xThis constitutes a group of first level gates.
xDraw a single gate using the AND-invert or the invert-OR graphic symbol in the second level, with inputs coming from outputs of first level gates.
xA term with a single literal requires an inverter in the first level. How ever if the single literal is complemented, it can be connected directly to an input of the second level NAND gate.

14.Give the general procedure for converting a Boolean expression in to multilevel NANDdiagram?
Draw the AND-OR diagram of the Boolean expression.
xConvert all AND gates to NAND gates with AND-invert graphic symbols.
xConvert all OR gates to NAND gates with invert-OR graphic symbols
Check all the bubbles in the same diagram. For every bubble that is not compensated by another circle along the same line, insert an inverter or complement the input literal.

PART-B

1. Simplify the Boolean function using K – map and implement using only NAND gates.
2. F (A, B, C, D) = ∑m (0, 8, 11, 12, 15) + ∑d (1, 2, 4, 7, 10, 14). Mark the essential and non – essential prime implicants. [Nov'15]
3. Give the general procedure for converting a Boolean expression in to multilevel NAND diagram. (Apr'18)
4. Simplify and implement the following SOP function using NOR gates f(A,B,C,D) = ∑ m(0,1,4,5,10,11,14,15) [May'12]
5. Reduce the following function using K-map, f(A,B,C,D) = π M(0,2,3,8,9,12,13,15) [Apr'15]
6. Express the function F=A+B'C in Canonical SOP form and Canonical POS form [Nov'13, Nov'17]
7. Using K-map simplify the following function and implement the function using logic gates f(A, B, C) = πM (0, 4, 6) [Nov'12]
8. Simplify the logical expression using K-map in SOP and POS form. F(A,B,C,D)=∑m(0,2,3,6,7)+d(8,10,11,15). (Nov'16)
9. Prove that for constructing XOR from NAND's we need 4 NAND gates. [May'13]
10. Implement the following Boolean function with NAND-NAND logic. Y = AC + ABC + A'BC + AB + D [May'12]
11. Write brief notes on the following: i) Demorgan's theorem ii) Comparators iii) Binary to gray code converter. [Nov'11]

12. Design a decimal adder to add two decimal digits [Apr'10]
13. Design a full adder using two half-adders and an or gate. [Apr'15]
14. Design a Full adder and implement it using suitable multiplexer. [May'16]
15. Design a full adder using only NOR gate. [May'17]
16. Explain Half Subtractor & Full Subtractor Circuit. [Nov'13, Nov'14]
17. Design a full subtractor and implement using logic gates. [Nov'15]
18. Design a full subtractor and realize using logic gates. Also implement the same using half subtractors. (Nov'16)
19. Design a 3x8 decoder and explain its operation as a minterm generator. [May'17]
20. Implement the function F (p, q, r, s) =Σ (0, 1, 2, 4, 7, 10, 11, 12) using Decoder. [Nov'14]
21. Implement the given function using Multiplexer F(x,y,z) = ∑(0,2, 6,7) [May'12]
22. Implement the following function f (A,B,C) = ∑ m(0,3,5) using 8:1 MUX. [Nov'12]
23. Implement the following function using a suitable multiplexer. F (a,b,c) = ∑m(3,7,4,5)

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS

PART-A

1. Define Flip flop.

- The basic unit for storage is flip flop.
- A flip-flop maintains its output state either at 1 or 0until directed by an input signal to change its state.
-

2. What are the different types of flip-flop?

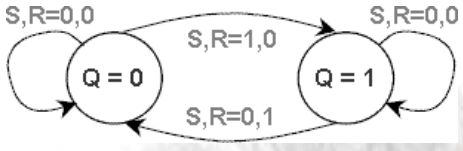
There are various types of flip flops. Some of them are mentioned below they are:

1. SR flip-flop,
2. D flip-flop,
3. JK flip-flop,
4. T flip-flop

3.Draw the truth table and state diagram of SR flip flop.

CLK	S	R	Qn	Qn+1	State
1 1	0 0	0 0	0 1	0 1	No Change (NC)
1 1	0 0	1 1	0 1	0 0	Reset

1 1	1 1	0 0	0 1	1 1	Set
1 1	1 1	1 1	0 1	x x	Indeterminate (*)



4. What is the drawback of SR flipflop?

- When we provide two input as 1 or true or high output of q and q' become same that violate the complement law.

5. Write the truth table of D flip-flop.

EN	D	Qn	Qn+1	State
1	0	X	0	Reset
1	1	X	1	Set
0	X	X	Qn	No Change (NC)

6. Define race around condition.[OR] What do you mean by race around condition in a flip flop?

- In JK flip-flop output is fed back to the input.
- Therefore change in the output results change in the input.
- Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously.
- This condition is called 'race around condition'.

7. What are the various types of triggering of flip-flop?

- Level triggering
  - o High level
  - o Low level
- Edge triggering
  - o Positive edge
  - o Negative edge

8. The JK flip-flop is a universal flip-flop. Justify.

- Using JK flip-flop we can construct other flip-flop like SR, D and T.
- So it is called as universal flip-flop.

9. **What is a master-slave flip-flop? Mention the major applications of Master Slave FF.**

- A master-slave flip-flop consists of two flip-flops, where first circuit serves as a master flip flop and other flip flops acts as a slave.
- The input is given to the first flip flop (Master) and the second flip flop (slave) onwards it must get the input from corresponding first one only.
- The master slave flip flop is used as a solution to the race around problem in flip flops.

10. Define registers.

- A register is a group of flip-flops; flip-flop can store one bit information.
- So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

11. Define shift registers.

- The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses.
- This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors.This gives rise to group of registers called shift registers.

12. What are the different types of shift registers?

There are five types.

1. Serial In Serial Out Shift Register
2. Serial In Parallel Out Shift Register
3. Parallel In Serial Out Shift Register
4. Parallel In Parallel Out Shift Register
5. Bidirectional Shift Register

13. Define Shift Register Counter.

- A shift register can also be used as a counter.
- A shift register with the serial output connection back to the serial input is called Shift register counter.

14. What are the two types of shift register counters?

There are 2 types of shift register counters:

i) Ring counter:

A ring counter is a circular shift register with only one flip flop being set, at any particular time, all others are cleared.

ii) Johnson counter:

The Johnson counter is a K-bit switch-tail ring counter with 2k decoding gates to provide outputs for 2ktiming signals.

15. What are the applications of shift register?

- Shift register act as sequence generator
- Used in delay lines.
- Used in counters.
- Used as a memory element.

16. What is bi-directional shift register and unidirectional shift register?

- A register capable of shifting both right and left directions are called as bi-directional shiftregister.
- A register capable of shifting only in one direction left or right directions are called unidirectional shift register.

17. Define sequential circuit? [Apr'10]

- In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past output of these input variables.

18. What are the classifications of sequential circuits?

- The sequential circuits are classified on the basis of timing of their signals into two types.

1) Synchronous sequential circuit.

2) Asynchronous sequential circuit.

PART-B

1. Explain the various types of triggering with suitable diagrams. Compare their merits and demerits. [Nov'14, Nov'17]

2. Explain the circuit of a SR flip-flop and explain its operation. [Nov'14]

3. Explain the operation of SR flip flop. (Apr'18)

4. Realize SR FF using NAND gates and explain its operations. [May'12]

5. Sketch the state diagram and state table for 'D' flip-flops. [Nov'12]

6. Sketch the state diagram and state table for JK' flip-flops. [Nov'12].

7. Explain the operation of JK flip flop (Apr'18)

8. Explain the operation of a Master-Slave JK Flip-flop. [Apr'15, May'16, May'17, Nov'17]

9. Explain the working principle of T FF. (OR) Explain the operation of T flip flop (Apr'18)

10. Explain the operation, state diagram and characteristics of T flip flop. (Nov'17)

11. Design a 4 bit parallel –in serial out shift register using D Flip Flops. [May'17]

12. Design a 3-bit bi-direction shift register. [Apr'15]

13. Design a Sequential logic circuit for a 3 bit binary counter. [Nov'12]

14. Design a 4-Bit Synchronous Decade Counter. [Nov'12] (BCD Counter).

15. Design a MOD-5 synchronous counter using JK Flip-Flops. [Apr'15]

16. Design a MOD5 counter using T flip flop. [May '16]

17. Design a 5 bit ring counter and mention its application. [May '17]

18. Design MOD 7 counter using D flip flop. [May'14]

19. Design a MOD-7 synchronous counter using JK Flip-Flops. Write excitation table and state table.[May'14]

20. Explain in detail the operation of a 3-Bit Asynchronous Binary Counter (OR) Binary ripple counter. [Nov'12]

21. Design an asynchronous modulo – 8 down counter using JK flip flop. [Nov'14]

22. Design an Asynchronous Decade (MOD 10) Counters. [Nov '12]

23. Design a counter with the sequence 0, 1, 3, 7, 6, 4, 0.[Nov'10]

24. Design synchronous sequential circuit that goes through the count sequence 1, 3, 4, 5 repeatedly. Use T flip-flops for your design. [Nov'14]

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES

PART-A

1. **Define asynchronous sequential machine.**

In asynchronous sequential circuits, no clock pulses and only the input variables are responsible for state change.

2. **What is meant by transition table?**

A state table with binary assignment is called transition table.Transition table of asynchronous sequential circuit is similar to table used for synchronous sequential circuits.It is constructed which shows the next states of flip-flops as a function of the present state and inputs.

3. **Define flow table in asynchronous sequential circuit.[OR]What is flow table? Give example.**

In asynchronous sequential circuit state table is known as flow table because of the behavior of the asynchronous sequential circuit.The stage changes occur independent of a clock, based on the logic propagation delay, and cause the state to flow from one to another.

4. What is the difference between flow table and transition table?

A state table with binary assignment is called transition table.It is constructed which shows the next states of flip-flops as a function of the present state and inputs. During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values.

Such a table is called flow table.

5. Define Race condition in Asynchronous sequential circuit? [OR]
Define races in asynchronous sequential circuits.

When two or more binary state variables change their value in response to a change in input variables, race condition occurs in asynchronous sequential circuit.In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

6. What is a deadlock condition?

In a counter, if the next state of some unused state is again in some unused state, it may happen that the counter remains in unused state, never to arrive at a used state.

Such condition is called a lockout condition or dead lock condition.

7. How can we avoid the lockout condition?

To avoid the lockout, the counter should be provided with an additional logic circuitry which will force the counter from an unused state to the next state as initial state.

8. What is Self-starting counter?

- The counter which16. What is write cycle time?

Two write cycle time is the minimum time for which an address must be held stable on the address bus, in write cycle.

9. Name types of Hazards. [OR] What are hazards in asynchronous sequential circuits? [OR] State the hazards in asynchronous sequential circuits?

A Hazard is a status where the output of the system is not what it should be i.e., it is temporarily false.

For example, an output which is supposed to be a '0' at an instant, but may occur as a '1'.

If this output is an input to another system, it may cause malfunction of the system.

Static hazard

Static-0 hazard

Static-1 hazard

Dynamic hazard

10. State the difference between static 0 and static 1 hazard.

STATIC-0 HAZARD STATIC-1 HAZARD

When the output is to remains at the value 0 and a momentary 1 output is possible, during the transition between the two input states.

Two input states both produce a 1 output steady state and a momentary 0 output is possible, during the transition between the two input states.

11. What is memory cycle?

Memory cycle is represented as read and write memory cycle with their timing parameters.

12. What is meant by memory expansion? Mention its limits?

The memory expansion can be achieved in two ways:

By expanding word size

By expanding memory capacity.

Limits: (i) The expansion of word size is limited by the data bus width.

(ii) The expansion of memory capacity is limited by address bus width.

What is meant by static and dynamic memories? Static memory:

Static RAM contains less memory cells per unit area.

Its access time is less hence faster memories. Static RAM consists of number of flip-flops.

Each flip-flop stores one - bit.

Refreshing Circuitry is not required. Cost is more.

Dynamic memory:

Dynamic RAM contains more memory cells as compared to static RAM per unit area.

Its access time is greater than static RAMs. Dynamic RAM stores the data as a change on the capacitor.

It consists of MOSFET and the capacitor for each cell. Refreshing Circuitry is required.

Cost is less.

13. Name the types of ROM.

There are four types of ROM:

Masked ROM

PROM

EPROM

EEPROM or E2PROM.

14. Whether ROM is classified as nonvolatile storage device? Why?

It is a read only memory.

We cannot write data in this memory.

It is non-volatile memory. (i.e.) it can hold data even if power is tuned off generally, ROM is used to store the binary codes for the sequence of instruction you want the computer to carry out and data such as look up tables.

This is because this type of information does not change.

15. What is a PROM?

PROM is Programmable Read Only Memory.

It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

16. How is individual location in an EEPROM Programmed or erased?

Since it is electrically erasable memory by activating particular row and column it is possible that individual can be programmed or erased.

17. Write the advantages of EPROM over PROM.

The important point is that we can erase the stored data in the EPROM by exposing the chip to ultraviolet light through its quartz window for 15 to 20 minutes.

18. What is PLA?

PLA stands for Programmable Logic Array, which is a LSI component.In PLA, both AND & OR gates have fuses at the input, therefore in PLA both AND & OR gates are programmable. The output from OR gates go through fuses as inputs to output inverters so that the final output can be programmed as either AND-OR or AND-OR-INVERT.

19. What is FGPA?

FGPA stands for field programmable gate array, which is the next generation in the programmable logic devices. The word field refers to the ability of the gate arrays to be programmed for a specific function by the end user. The word array indicates a series of columns and rows of gates that can be programmed by the end user.

20. List the configurable elements in the FGPA architecture.

The FGPA architecture consists of three types of configurable elements:

A perimeter of input/output blocks (IOBs).

A core array of configurable logic blocks (CLBs).

Resources for interconnection.

21. What is static hazards and dynamic hazard?

Static hazard:

A static hazard is the situation where, when one input variable changes, the output changes momentarily before stabilizing to the correct value.

There are two types of static hazards:

Static-1 Hazard: the output is currently 1 and after the inputs change, the output momentarily changes to 0,1 before settling on 1

Static-0 Hazard: the output is currently 0 and after the inputs change, the output momentarily changes to 1,0 before settling on 0

Dynamic hazard:

A dynamic hazard is the possibility of an output changing more than once as a result of a single input change.Dynamic hazards often occur in larger logic circuits where there are different routes to the output (from the input)

22. What are the two types of asynchronuous sequential circuits?

Fundamental mode asynchronuous sequential circuits

Pulse mode asynchronuous sequential circuits.

23. Define address and word.

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

24. Why was PAL developed?

It is a PAL that was developed to overcome certain disadvantage of PLA such as longer delays due to additional fusible links that result from using two programmable arrays and more circuits complexity.

The development of a PAL involves research about how storage information in different formats and multiple purpose and it is priority to know how package and transfer process knowledge as corporate assets.

PART-B

1. Derive the transition table and primitive flow table for the functional mode asynchronous sequential circuit. [Nov' 2013]
2. Consider the following asynchronous sequential circuit and draw maps and transition table and state table. [May' 2013]
3. Illustrate the analysis procedure of asynchronous sequential circuit with an example. [May'13]
4. What are transition table and flow table? Give Suitable examples. [May'16]
5. Discuss the steps involved in the design of an asynchronous sequential circuit with a suitable example. [Nov'12]
6. Describe the steps involved in design of asynchronous sequential circuit in detail with an example. [Apr'11]
7. 14. Find a circuit that has no static hazards and implements Boolean function F(A,B,C,D) = Σ(0,2,6,7,8,10,12) [May'14]
8. 15. Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples. [Nov'14]
9. 16. What is hazards? Explain hazards in digital circuits? (Nov'17)
10. 17. Describe with reason, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race – Free State assignments with examples. [Nov'14]
11. 18. Explain cycles and races in asynchronous sequential circuits. [May '16]
12. 19. What are static -0 and static -1 hazards? Explain the removal of hazards using hazard covers in k-map? (May '16)
13. 20. Discuss about hazards in asynchronous sequential circuit and the ways to eliminate them.
14. (Nov'17)
15. 21. For the given Boolean function, obtain the hazard – free circuit. F (A,B,C,D) = Σm (1,3,6,7,13,15). [Apr'15]
16. Implement the following logic and analyse for the pressure of any hazard F=$x1x2 + x1x3$.If hazard is present briefly explain the type of hazard and design a hazard –free circuit. (May'17)
17. When do you get the critical and non-critical races? How will you obtain race free condition?
18. [Apr'10]
19. Design an asynchronous BCD counter. [Apr'11, May'14]

20. Describe the characteristics of all types of memories. [Apr'11]
21. Describe the different types of memories. [Apr'10, May'14]
22. Explain the operation of bipolar RAM cell with suitable diagrams. (Apr'18)
23. Write notes on ROM and its types. [May'12]
24. Elaborate the concept of PROM, EPROM, EEPROM in detail. (Apr'18)
25. Write briefly about the programmable logic array and EPROM. [Nov'11]
26. Describe the working of EPROM. List the application EPROM.
27. Illustrate the basic principles of PLA and FPGA. [May'13]
28. Write short note on field programmable gate Array (FPGA).
29. Describe the concept and working of FPGA. [May'12]
30. What do you understand by FPGA? Explain the operation and applications? [Nov'10]
31. Write short notes on PLA and PAL. (Nov'17)
32. Design ROM for the following functions.F1 = ∑(1,2,3); F2 = ∑(0,2) [Apr'11]
33. Implement the following two Boolean functions with a PLA? a. F1 (A,B,C) = ∑ (0,1,2,4)
34. b. F2 (A,B,C) = ∑ (0,5,6,7)[Apr'11]
35. Implement the following function using PLA: F(x,y,z) = ∑m(1, 2, 4, 6). [Apr'15]
36. Implement the following function using PLA. F1(x,y,z)=∑m(0,1,3,5,7), F2(x,y,z)=∑m(2,4,6).
37. (May'17)
38. Design and implement a 4-bit binary to gray code converter using a PLA. [Nov'12]
39. Design an AND-OR-PLA that implements the functions. f (x, y, z) = ∑m(0,2,4,6) 43. g (x, y, z) = ∑m(1,3,5,7) [Nov'12]
40. Design a PLA structure using AND and OR logic for the following functions. F1=∑m(0,1,2,3,4,7,8,11,12,15), F2=∑m(2,3,6,7,8,9,12,13), F3=∑m(1,3,7,8,11,12,15), F4=∑m(0,1,4,8,11,12,15)(Nov'16)
41. Implement the following function using PLA and PAL. F(x,y,z) = ∑m(0,1,3,5,7). (May '16)
42. 46. Design a combinational circuit using ROM. The circuit accepts 3-bit number and generates an output binary number equal to square of input number. [Apr'10]
43. 47. Show how to program the fusible links to get a 4 bit Gray code from the Binary inputs using PLA and PAL and compare the design requirements with PROM. [Nov'15]

UNIT V VHDL

PART-A

1. **What is the need for VHDL?**

   VHDL represents' digital systems in the form of documentation which can be understood by human as well as computers.

It makes easy to exchange the idea between the designers.

VHDLs are used to describe hardware for the purpose of simulation, modeling, testing, and documentation.

It allows the designer to express their design with behavioral constructs.

2. **What are the main components of a VHDL description?**

- The main components of a VHDL description consists of following kinds of declarations
- Package (optional)
- Entity
- Architecture
- Configuration (optional)

3. **What is entity?**

- Entity gives the specification of input/output signal to external circuitry. It gives interfacing between device and the other peripherals. An entity usually has one or more ports, which are analogous to the pins on a schematic symbol.
- All information must flow into and out of the entity through the ports. Each port must contain name, data flow direction and type.

4. **What is architecture?**

- Architecture specifies behavior, functionality, interconnections or relationship between inputs and outputs.
- It is the actual description of the design. Architecture consists of two portions: architecture declaration and architecture body.

5. **How is package represented?**

A package is represented by:

- Package declaration
- Package body (optional)

6. What is a package in VHDL?

- There are some declarations which are common across many design units.
- A package is a convenient mechanism to store and share such declarations.
- A set of declarations contained in a package declaration may be shared by many design units.
- It defines items that can be made visible to other design units.

7. State the advantages of package declaration in VHDL over component declaration.

[Nov'14]

- Component declarations are in the package.
- Do not have to be declared in the architecture.
- They occur in the package header
- Necessary to compile the package components prior to compiling the entity comparator since the use statement refers to something that already exists in the library.

8. What is behavior modeling?

- The modeling style which directly describes the behavior of the functionality of a circuit is called behavioral modeling.
- It is very similar in syntax and semantics to that of a high-level programming language (for example: C, Pascal). A behavioral description models the system as to how the outputs behave with the inputs.

9. What is data flow modeling?

- Data flow describes how the circuit signals flow from the inputs to the outputs.
- There are some concurrent statements which allow to describe the circuit I terms of operations on signals and flow of signals in the circuit.

- When such concurrent statements are used in a program, the style is called a dataflow modeling.

10. What is structural modeling?

- The modeling style which uses components or gates to model the system is called structural modeling.

11. List the different type of operators supported by VHDL.

1. Logical Operator NOT, AND, OR, NAND, NOR & XOR
2. Arithmetic Operator +, –, *, &, /

12. List the different types of test benches?

The different type of test benches are:

1. Stimulus only
2. Full test bench
3. Simulator specific
4. Hybrid test-bench
5. Fast test bench

13. What is the meaning of the following RTL statement?

- The contents of register ACC are bitwise ANDed with the contents of MDR register and the result is stored in the ACC register when control signal T1 is activated.

14. Write the VHDL code for AND gate? [OR] Write the VHDL code for AND gate? [OR] Write the VHDL code for a logical gate which gives high output only when both the input are high.

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity and gate is
port (A, B: in std_logic); Y: out std_logic);
```

end and gate;

architecture arch_and of and gate is begin

Y <= A and B;

end;

3. Relational Operators □ =, /=, <, <=, >, >=
4. Concatenation Operator

15. Give the classification of data types supported by VHDL.

The VHDL data types can be broadly classified into following five data types:

i. Scalar types: the scalar types include numeric data types and enumerated data types. The numeric types consist of integer, floating point (real) and physical types. Bit, Boolean and character are all enumerated types.

ii. Composite types: array and record types are composite data types. The values of these types are collection of heir elements.

iii. Access types: they are pointers; they provide access to objects of a given data type.

iv. File type: they provide access to object that contain a sequence of values of a given type.

v. Other types: they include the data types provided by the several external libraries.

PART-B

1. Write the VHDL code for mod 6 counters? (Apr'10, Apr'11, May'12)
2. Explain the structural VHDL description for a 2 to 4 decoder in details.(Nov'13)
3. Write HDL for four bit binary counter with parallel load and explain. Description of a 4 bit synchronous counter with parallel load. (May'13)
4. Write HDL for two to one quadruple multiplexer with dataflow description and behavioral description.(May'13)
5. Briefly discuss the different data types supported in VHDL. (Nov'12)
6. Write an HDL code that implements an 8:1 multiplexer (Nov'12, May'14)
7. Design a 4x4 array multipler and write the VHDL code to realize it using structural modeling. [May'17]
8. Briefly discuss the use of 'packages' in VHDL. (Nov'12)
9. Discuss briefly the packages in VHDL. (Nov'17)

10. Write a VHDL program and explain the design procedure of 8 bit comparator. (Nov'13)
11. Write a VHDL code for a 4-bit universal shift register. [Nov'14]
12. Write the VHDL code to realize a 3-bit Gray code counter using case statement. [Apr'15]
13. Write a VHDL Program for 1 to 4 Demux using dataflow modeling. [Nov'15]
14. VHDL Behavioral description of 2 x 1 multiplexer. [May'16]
15. Write the VHDL code to realize a decade counter with behavioural modeling.[May'16]
16. Write VHDL coding for 4x1 Multiplexer. [Nov'16, Nov'17]
17. Write short note on built in operators used in VHDL programming. [Nov'16]
18. Explain functions and subprograms with suitable examples. [May'16]
19. Write a VHDL coding for realization of clocked SR flip flop. (Nov'17)

END